REMARKS

Claims 29 and 33-35 remain in this application. Claims 30-32 have been canceled. Claims 29, 33-35 have been amended.

Examiner S. Loke is thanked for having thoroughly examined the present invention.

A drawing sheet for Fig. 1 showing a correction in the form of pen-and-red ink is submitted for examiner's approval.

As for the informalities, the phrase "said oxide liner" in claim 29, lines 29-30 has been amended to read "said oxide layer" and "said intergate oxide" has been amended to read "said intergate oxide layer", thereby both phrases having the proper antecedence. Also, claims 33-35 have been amended to indicate clearly that the references are to "claim 29". It is believed that objections now have been overcome, and it is so requested, respectfully.

Reconsideration of the rejection of claim 29 under 35 USC 102(e)as being clearly anticipated by Doan is respectfully

requested in view of the amendments and for the reasons given below.

Firstly, it is assumed that the reference to Doan is to US Patent No. 6,271,561, and not to US Patent No. 6,054,733 of the previous office action.

Secondly, the applicants respectfully disagree with the examiner that Doan "shows all the elements of the claimed invention in Figures 1A-8. For Doan never shows anywhere " a floating gate having folding surfaces." In the cross-sectional views Figs. 1F, 1G and 5A of the reference, it is clearly seen that the conductive layer 36A which becomes floating gate 50, has flat bottom and top surfaces without any folded surfaces of the instant invention. Likewise, control gate 28 of the reference is flat both at the bottom and the top. Doan states unequivocally that first conductive layer 36A is planarized flat using chemical mechanical polishing to form floating gates (column 6, lines 20-21, and claim 1, lines 46-48). The same also holds true for the control gate as cited in the column, lines 55-59.

In contrast, in the instant invention, floating gate 270 and control gate 290, including the intervening intergate oxide

layer 280 all have folding surfaces, which overlay each other conformally, as shown in Figure 3e. The structure of the present invention provides several-fold coupling area between the floating gate and the control gate due to the higher and several folding interior walls of the floating gate formed against the high-step oxide protruding over the shallow trench isolation of the present invention (pages 19-20). Doan does not anticipate multiple folding surfaces, and it is believed that the instant invention is clearly distinguishable, and patentable over Doan, and it is so requested, respectfully.

Reconsideration of the rejection of claims 33-35 under 35 USC 103(a) as being unpatentable over Doan is respectfully requested in view of the amendments and for the reasons given below.

It is respectfully submitted that claim 29, from which claims 33-35 depend, is allowable for the reasons given above and reiterated here. Doan never shows anywhere " a floating gate having folding surfaces." In the cross-sectional views Figs. 1F, 1G and 5A of the reference, it is clearly seen that the conductive layer 36A which becomes floating gate 50, has flat bottom and top surfaces without any folded surfaces of the instant invention. Likewise, control gate 28 of the reference is flat both at the bottom and the top. Doan states

unequivocally that first conductive layer 36A is planarized flat using chemical mechanical polishing to form floating gates (column 6, lines 20-21, and claim 1, lines 46-48). The same also holds true for the control gate as cited in the column, lines 55-59.

In contrast, in the instant invention, floating gate 270 and control gate 290, including the intervening intergate oxide layer 280 all have folding surfaces, which overlay each other conformally, as shown in Figure 3e. The structure of the present invention provides several-fold coupling area between the floating gate and the control gate due to the higher and several folding interior walls of the floating gate formed against the high-step oxide protruding over the shallow trench isolation of the present invention (pages 19-20).

It is respectfully suggested that the cited reference cannot be obvious without reference to the applicants' own invention. It is believed that the cited reference does not offer multiply folded floating gate to increase several-fold the coupling between of the floating gate. The applicants have claimed the disclosed structure in detail. Figs. 2a-2f, 3a-3g (Claims 29, 33-35) are believed to be novel and patentable over the Doan reference because there is not sufficient basis for

concluding that the claimed elements would have been obvious to one skilled in the art. It is believed that independant claim 29, and claims 33-35 dependent from claim 29, as amended, are allowable, and we therefore request respectfully that examiner Steven Ho Yin Loke reconsider this rejection in view of these arguments and the amendments to the claims.

Allowance of all claims, as amended, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Marking to Show Changes Made.**"

It is requested that should the Examiner not find that the Claims Allowable that are now presented, that he call the undersigned Attorney at 845/452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 29, 33-35 have been amended as follows:

29. (AMENDED) A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:

a substrate having a gate oxide layer;

at least two trenches formed to a depth between about 2500 to 5000 Å below the surface of said substrate;

an oxide layer formed over said substrate, including over the inside walls of said two trenches;

a high-step oxide formed within said two trenches over said oxide [liner] <u>layer</u> and protruding upward over the surface of said substrate to a height between about 2000 to 6000 Å;

said high-step oxide forming an opening with high walls over the surface of said substrate between said two trenches;

a first conductive layer formed conformally inside said opening and over the surface of the substrate between said high walls to form a floating gate having folding surfaces;

an intergate oxide layer formed over said floating gate having folding surfaces;

a second conductive layer formed protruding downward in between said folding surfaces over said intergate oxide layer to form a control gate; and

a self-aligned source (SAS) line.

33. (AMENDED) The stacked-gate flash memory cell of claim 29, wherein said opening has a width between about 1500 to 5000 Å.

34. (AMENDED) The stacked-gate flash memory cell of claim 29, wherein said first conductive layer is polysilicon having a thickness between about 100 to 500 Å.

35. (AMENDED) The stacked-gate flash memory cell of claim 29, wherein said second conductive layer is polysilicon having a thickness between about 1000 to 3000